MS power

MS POWER GmbH

Application note

# Distributed Gate Thyristors for Induction Power Supply Applications

MS Power has accumulated valuable expertise in the design and manufacturing of Distributed gate thyristors for Induction power supplies for Melting, Surface conditioning, Billet heating. Concurrent engineering with leading induction power supplies manufacturers has resulted in continuous improvements and led to the design of industry standard package offering higher current density and improved turn-off characteristics.

Features:

- High di/dt
- High average current rating
- Low thermal resistance
- Fully hermetic, industry standard packages
- Double side cooling
- Higher surge current rating

Application includes:

- Resonant power supplies
- Induction power supplies for
  Melting
  Surface conditioning
  Billet heating
- Inverters

# Contents

## MS Power Distributed Gate Thyristors

MS Power has been cooperating with most of the major Induction power supplies manufacturers. Through this cooperation, MS Power has gathered experience in the utilization of thyristors to reach optimal reliability and electrical performance. These devices are available with blocking voltage to 2.8kV, average current to 4.0kA and Tq from 12 to 100µsec.

The features like distributed gate design and lifetime control results in both high di/dt capability and fast, low recovery turn off, while maintaining a low on-state voltage drop.

The product range of MS Power distributed gate thyristors is shown in table 1. Actual device data sheets are available at the web site www.mspowergroup.com.

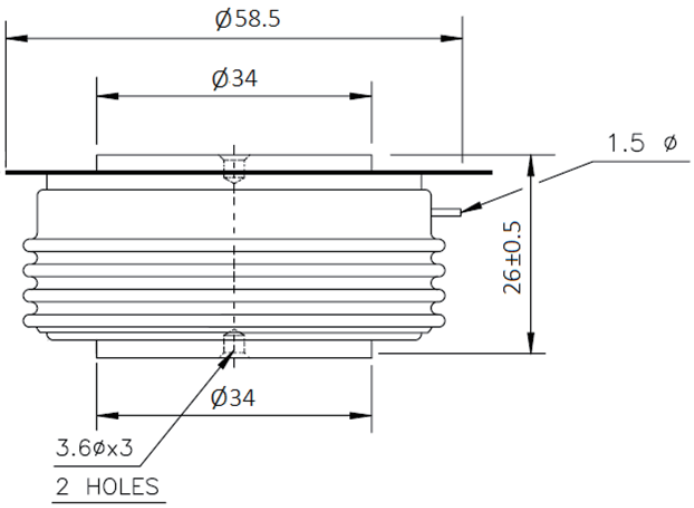
Product Range :

| Type | $V_{DRM}$,$V_{RRM}$ [V] $V_{DSM}=V_{DRM}$ $V_{RSM}=V_{RRM}+100V$ | $I_{TAVM}$ / $T_C$ [A / °C] @ 180° Sine DSC | $I_{TSM}$ [kA] @ 10ms $T_{jmax}$ | $\int i^2t$ [$A^2S \times 10^3$] @ 10ms $T_{jmax}$ | $V_{(TO)}$ [V] @$T_{jmax}$ | $r_T$ [mΩ] @$T_{jmax}$ | Tq [µsec] @$T_{jmax}$ | (di/dt)crit [A/µs] @$T_{jmax}$ | $R_{thJC}$ [°C/W] @ 180° Sine DSC | $T_{jmax}$ [ °C] | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MS TF800C10HE | 1000 | 800 / 73 | 9.1 | 414 | 2.1 | 0.300 | 15 | 500 | 0.024 | 125 | 1 |
| MS TF800C10HK | 1000 | 800 / 73 | 9.1 | 414 | 2.1 | 0.300 | 20 | 500 | 0.024 | 125 | 1 |
| MS TF800C10HJ | 1000 | 800 / 73 | 9.1 | 414 | 2.1 | 0.300 | 25 | 500 | 0.024 | 125 | 1 |
| MS TF800C14HE | 1400 | 800 / 73 | 9.1 | 414 | 2.1 | 0.300 | 15 | 500 | 0.024 | 125 | 1 |
| MS TF800C14HK | 1400 | 800 / 73 | 9.1 | 414 | 2.1 | 0.300 | 20 | 500 | 0.024 | 125 | 1 |
| MS TF800C14HJ | 1400 | 800 / 73 | 9.1 | 414 | 2.1 | 0.300 | 25 | 500 | 0.024 | 125 | 1 |
| MS TF980C08FK | 800 | 980 / 73 | 11.0 | 605 | 1.320 | 0.360 | 20 | 1200 | 0.024 | 125 | 1 |
| MS TF980C08FJ | 800 | 980 / 73 | 11.0 | 605 | 1.320 | 0.360 | 25 | 1200 | 0.024 | 125 | 1 |
| MS TF980C08FN | 800 | 980 / 73 | 11.0 | 605 | 1.320 | 0.360 | 30 | 1200 | 0.024 | 125 | 1 |
| MS TF980C08F2J | 800 | 980 / 73 | 11.0 | 605 | 1.320 | 0.360 | 50 | 1200 | 0.024 | 125 | 1 |
| MS TF980C12FK | 1200 | 980 / 73 | 11.0 | 605 | 1.320 | 0.360 | 20 | 1200 | 0.024 | 125 | 1 |
| MS TF980C12FJ | 1200 | 980 / 73 | 11.0 | 605 | 1.320 | 0.360 | 25 | 1200 | 0.024 | 125 | 1 |
| MS TF980C12FN | 1200 | 980 / 73 | 11.0 | 605 | 1.320 | 0.360 | 30 | 1200 | 0.024 | 125 | 1 |
| MS TF980C12F2J | 1200 | 980 / 73 | 11.0 | 605 | 1.320 | 0.360 | 50 | 1200 | 0.024 | 125 | 1 |
| MS TF1000C14H2J | 1400 | 1000 / 77 | 18.5 | 1711 | 1.207 | 0.342 | 50 | 250 | 0.023 | 125 | 2 |
| MS TF1000C14H4J | 1400 | 1000 / 77 | 18.5 | 1711 | 1.207 | 0.342 | 100 | 250 | 0.023 | 125 | 2 |
| MS TF1000C18H2J | 1800 | 1000 / 77 | 18.5 | 1711 | 1.207 | 0.342 | 50 | 250 | 0.023 | 125 | 2 |
| MS TF1000C18H4J | 1800 | 1000 / 77 | 18.5 | 1711 | 1.207 | 0.342 | 100 | 250 | 0.023 | 125 | 2 |
| MS TF1000C20H2J | 2000 | 1000 / 77 | 18.5 | 1711 | 1.207 | 0.342 | 50 | 250 | 0.023 | 125 | 2 |
| MS TF1000C20H4J | 2000 | 1000 / 77 | 18.5 | 1711 | 1.207 | 0.342 | 100 | 250 | 0.023 | 125 | 2 |
| MS TF1271C08FK | 800 | 1271 / 72 | 20.0 | 2000 | 1.540 | 0.240 | 20 | 1200 | 0.018 | 125 | 2 |
| MS TF1271C08FJ | 800 | 1271 / 72 | 20.0 | 2000 | 1.540 | 0.240 | 25 | 1200 | 0.018 | 125 | 2 |
| MS TF1271C08FN | 800 | 1271 / 72 | 20.0 | 2000 | 1.540 | 0.240 | 30 | 1200 | 0.018 | 125 | 2 |
| MS TF1271C08F2J | 800 | 1271 / 72 | 20.0 | 2000 | 1.540 | 0.240 | 50 | 1200 | 0.018 | 125 | 2 |
| MS TF1271C12FK | 1200 | 1271 / 72 | 20.0 | 2000 | 1.540 | 0.240 | 20 | 1200 | 0.018 | 125 | 2 |
| MS TF1271C12FJ | 1200 | 1271 / 72 | 20.0 | 2000 | 1.540 | 0.240 | 25 | 1200 | 0.018 | 125 | 2 |
| MS TF1271C12FN | 1200 | 1271 / 72 | 20.0 | 2000 | 1.540 | 0.240 | 30 | 1200 | 0.018 | 125 | 2 |
| MS TF1271C12F2J | 1200 | 1271 / 72 | 20.0 | 2000 | 1.540 | 0.240 | 50 | 1200 | 0.018 | 125 | 2 |
| MS TF1275C18F2J | 1800 | 1275 / 70 | 17.5 | 1531 | 1.202 | 0.340 | 50 | 250 | 0.019 | 125 | 2 |

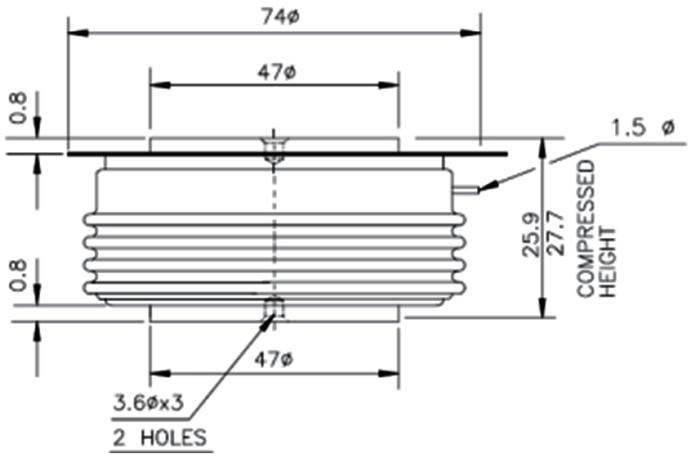
| Type | $V_{DRM}$, $V_{RRM}$ [V] $V_{DSM}=V_{DRM}$ $V_{RSM}=V_{RRM}+100V$ | $I_{TAVM}$ / $T_C$ [A / °C] @ 180° Sine DSC | $I_{TSM}$ [kA] @ 10ms $T_{jmax}$ | $\int i^2t$ [$A^2S$ X $10^3$] @ 10ms $T_{jmax}$ | $V_{(TO)}$ [V] @$T_{jmax}$ | $r_T$ [mΩ] @$T_{jmax}$ | Tq [µsec] @$T_{jmax}$ | (di/dt)crit [A/µs] @$T_{jmax}$ | $R_{thJC}$ [°C/W] @ 180° Sine DSC | $T_{jmax}$ [ °C] | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MS TF1275C18F2N | 1800 | 1275 / 70 | 17.5 | 1531 | 1.202 | 0.340 | 60 | 250 | 0.019 | 125 | 2 |
| MS TF1275C21F2J | 2100 | 1275 / 70 | 17.5 | 1531 | 1.202 | 0.340 | 50 | 250 | 0.019 | 125 | 2 |
| MS TF1275C21F2N | 2100 | 1275 / 70 | 17.5 | 1531 | 1.202 | 0.340 | 60 | 250 | 0.019 | 125 | 2 |
| MS TF2100C14H2N | 1400 | 2100 / 70 | 33.0 | 5445 | 1.271 | 0.255 | 60 | 300 | 0.010 | 125 | 3 |
| MS TF2100C14H4J | 1400 | 2100 / 70 | 33.0 | 5445 | 1.271 | 0.255 | 100 | 300 | 0.010 | 125 | 3 |
| MS TF2100C18H2N | 1800 | 2100 / 70 | 33.0 | 5445 | 1.271 | 0.255 | 60 | 300 | 0.010 | 125 | 3 |
| MS TF2100C18H4J | 1800 | 2100 / 70 | 33.0 | 5445 | 1.271 | 0.255 | 100 | 300 | 0.010 | 125 | 3 |
| MS TF2100C20H2N | 2000 | 2100 / 70 | 33.0 | 5445 | 1.271 | 0.255 | 60 | 300 | 0.010 | 125 | 3 |
| MS TF2100C20H4J | 2000 | 2100 / 70 | 33.0 | 5445 | 1.271 | 0.255 | 100 | 300 | 0.010 | 125 | 3 |
| MS TF2620C20F2J | 2000 | 2620 / 74 | 37.2 | 6919 | 1.308 | 0.170 | 50 | 1000 | 0.008 | 125 | 3 |
| MS TF2620C20F2N | 2000 | 2620 / 74 | 37.2 | 6919 | 1.308 | 0.170 | 60 | 1000 | 0.008 | 125 | 3 |
| MS TF2620C20F2G | 2000 | 2620 / 74 | 37.2 | 6919 | 1.308 | 0.170 | 70 | 1000 | 0.008 | 125 | 3 |
| MS TF2620C25F2J | 2500 | 2620 / 74 | 37.2 | 6919 | 1.308 | 0.170 | 50 | 1000 | 0.008 | 125 | 3 |
| MS TF2620C25F2N | 2500 | 2620 / 74 | 37.2 | 6919 | 1.308 | 0.170 | 60 | 1000 | 0.008 | 125 | 3 |
| MS TF2620C25F2G | 2500 | 2620 / 74 | 37.2 | 6919 | 1.308 | 0.170 | 70 | 1000 | 0.008 | 125 | 3 |
| MS TF3050C20F2K | 2000 | 3050 / 74 | 55.0 | 15125 | 1.320 | 0.140 | 40 | 1200 | 0.007 | 125 | 4 |
| MS TF3050C20F2J | 2000 | 3050 / 74 | 55.0 | 15125 | 1.320 | 0.140 | 50 | 1200 | 0.007 | 125 | 4 |
| MS TF3050C20F2N | 2000 | 3050 / 74 | 55.0 | 15125 | 1.320 | 0.140 | 60 | 1200 | 0.007 | 125 | 4 |
| MS TF3050C20F2G | 2000 | 3050 / 74 | 55.0 | 15125 | 1.320 | 0.140 | 70 | 1200 | 0.007 | 125 | 4 |
| MS TF3050C20F4J | 2000 | 3050 / 74 | 55.0 | 15125 | 1.320 | 0.140 | 100 | 1200 | 0.007 | 125 | 4 |
| MS TF3050C22F2K | 2200 | 3050 / 74 | 55.0 | 15125 | 1.320 | 0.140 | 40 | 1200 | 0.007 | 125 | 4 |
| MS TF3050C22F2J | 2200 | 3050 / 74 | 55.0 | 15125 | 1.320 | 0.140 | 50 | 1200 | 0.007 | 125 | 4 |
| MS TF3050C22F2N | 2200 | 3050 / 74 | 55.0 | 15125 | 1.320 | 0.140 | 60 | 1200 | 0.007 | 125 | 4 |
| MS TF3050C22F2G | 2200 | 3050 / 74 | 55.0 | 15125 | 1.320 | 0.140 | 70 | 1200 | 0.007 | 125 | 4 |
| MS TF3050C22F4J | 2200 | 3050 / 74 | 55.0 | 15125 | 1.320 | 0.140 | 100 | 1200 | 0.007 | 125 | 4 |
| MS TF3050C25F2K | 2500 | 3050 / 74 | 55.0 | 15125 | 1.320 | 0.140 | 40 | 1200 | 0.007 | 125 | 4 |
| MS TF3050C25F2J | 2500 | 3050 / 74 | 55.0 | 15125 | 1.320 | 0.140 | 50 | 1200 | 0.007 | 125 | 4 |
| MS TF3050C25F2N | 2500 | 3050 / 74 | 55.0 | 15125 | 1.320 | 0.140 | 60 | 1200 | 0.007 | 125 | 4 |
| MS TF3050C25F2G | 2500 | 3050 / 74 | 55.0 | 15125 | 1.320 | 0.140 | 70 | 1200 | 0.007 | 125 | 4 |
| MS TF3050C25F4J | 2500 | 3050 / 74 | 55.0 | 15125 | 1.320 | 0.140 | 100 | 1200 | 0.007 | 125 | 4 |
| MS TF4000C20F2J | 2000 | 4000 / 70 | 72.0 | 25920 | 1.450 | 0.360 | 50 | 1200 | 0.005 | 125 | 5 |
| MS TF4000C20F2N | 2000 | 4000 / 70 | 72.0 | 25920 | 1.450 | 0.360 | 60 | 1200 | 0.005 | 125 | 5 |
| MS TF4000C20F2G | 2000 | 4000 / 70 | 72.0 | 25920 | 1.450 | 0.360 | 70 | 1200 | 0.005 | 125 | 5 |
| MS TF4000C24F4J | 2400 | 4000 / 70 | 72.0 | 25920 | 1.450 | 0.360 | 100 | 1200 | 0.005 | 125 | 5 |
| MS TF4000C24F2J | 2400 | 4000 / 70 | 72.0 | 25920 | 1.450 | 0.360 | 50 | 1200 | 0.005 | 125 | 5 |
| MS TF4000C24F2N | 2400 | 4000 / 70 | 72.0 | 25920 | 1.450 | 0.360 | 60 | 1200 | 0.005 | 125 | 5 |
| MS TF4000C24F2G | 2400 | 4000 / 70 | 72.0 | 25920 | 1.450 | 0.360 | 70 | 1200 | 0.005 | 125 | 5 |
| MS TF4000C24F4J | 2400 | 4000 / 70 | 72.0 | 25920 | 1.450 | 0.360 | 100 | 1200 | 0.005 | 125 | 5 |
| MS TF4000C28F2J | 2800 | 4000 / 70 | 72.0 | 25920 | 1.450 | 0.360 | 50 | 1200 | 0.005 | 125 | 5 |
| MS TF4000C28F2N | 2800 | 4000 / 70 | 72.0 | 25920 | 1.450 | 0.360 | 60 | 1200 | 0.005 | 125 | 5 |
| MS TF4000C28F2G | 2800 | 4000 / 70 | 72.0 | 25920 | 1.450 | 0.360 | 70 | 1200 | 0.005 | 125 | 5 |
| MS TF4000C28F4J | 2800 | 4000 / 70 | 72.0 | 25920 | 1.450 | 0.360 | 100 | 1200 | 0.005 | 125 | 5 |

MS Power Semiconductor offers five different sizes of encapsulated thyristors. The outlines of five different housings are presented below. All dimensions are given in millimetres.

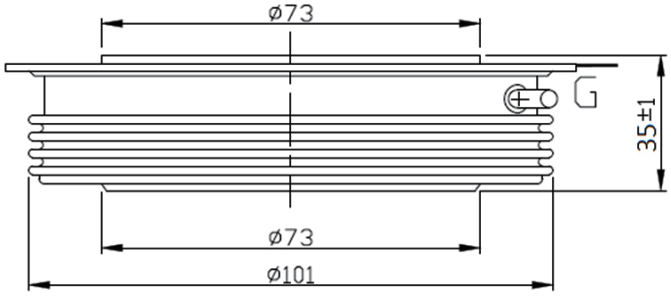
## Outline. 1



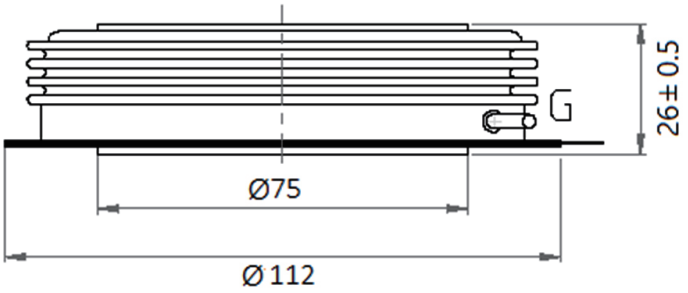

## Outline.2



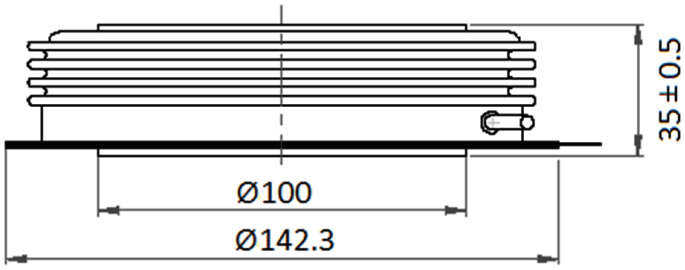

## Outline.3




## Outline.4




## Outline.5




This devices are constructed using an diffused silicon slice, fused to a metal disc, encapsulated in an industry standard package offering higher current density and improved turn-off characteristics. The thermal characteristics of the metal disc and its direct fusion to the silicon slice enhances performance, presenting excellent transient thermal characteristics and higher surge current ratings, as seen by device in resonant power supplies during difficult environment.

Figure A: Distributed gate thyristor housing and inside chip

To meet the application demand, MS Power offered Fast switching thyristors with $Q_{RR}/Q_{RA}$ in the band of ± 10% which greatly improve the balancing of voltage among thyristors connected in series at turn off.

## 2. data sheet user guide

The aim of this section is to guide readers through the distributed gate thyristor data sheet to understand it properly. The various device parameters which appear in the data sheet are defined and their dependencies are supported by figures where it is appropriate. For explanation purposes, data and diagrams associated with MSKK2620C24 are used. However, the guide is applicable to all the product range of distributed gate thyristors(table 1). The parameters are defined according to the standard IEC 60747.

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# MS TF2620

### Features

- Full blocking capability over wide temperature range
- High Surge current capability
- Hermetic metal case with ceramic insulator
- Distributed gate

### Key parameters

| | |
|---|---|
| $V_{DRM}$ / $V_{RRM}$ | = 2500V |
| $I_{T(AV)}$ | = 2620A |
| $I_{TSM}$ | = 38KA |
| $V_{T(TO)}$ | = 1.308V |
| $r_T$ | = 0.17mΩ |

The key parameters determine the basic voltage and current rating of the thyristors. The parameter values are followed by short descriptions of the main features of the thyristor.

Ordering Information

| MS TF | 2620 | C | X X | F | 2N |
|---|---|---|---|---|---|
| Fast Switching Thyristor | Current Code | Capsule Package With Alloyed Silicon Technology | Voltage Code Code X 100 = $V_{DRM}$/$V_{RRM}$ | Reapplied dv/dt F = 200V/usec | Turn off time code 2J = 50usec 2N = 60uesc 2G = 70usec |
| Order Code MS TF2620C20F2N - 2000V $V_{DRM}$,$V_{RRM}$,$T_q$=60usec,35mm clamp height capsule | | | | | |

Main features followed by ordering information.

### 2.1 Blocking

| | | | | | |
|---|---|---|---|---|---|
| $V_{RRM}$ | Repetitive peak reverse voltage | | 125 | 2000 - 2500 | V |
| $V_{RSM}$ | Non-repetitive peak reverse voltage | | 125 | 2100 - 2600 | V |
| $V_{DRM}$ | Repetitive peak off-state voltage | | 125 | 2000 - 2500 | V |
| $I_{RRM}$ | Repetitive peak reverse current | V = $V_{RRM}$ | 125 | 250 | mA |
| $I_{DRM}$ | Repetitive peak off-state current | V = $V_{DRM}$ | 125 | 250 | mA |

$V_{DRM}$: The maximum allowable forward off state voltage that may be applied to the thyristor repetitively. The thyristor must be operated at or below $V_{DRM}$. Above this level the device will thermally " run-away" and become a short circuit. The rating of $V_{DRM}$ is valid across the full operation temperature range of thyristor. The parameter is measured with 10ms half sine wave pulse and a repetition frequency of 50Hz.

$V_{RRM}$: The maximum allowable reverse voltage that may be applied to the thyristor repetitively. The thyristor must be operated at or below $V_{RRM}$. Above this level the device will thermally " run-away" and become a short circuit. The rating of $V_{RRM}$ is valid across the full operation temperature range of thyristor. The parameter is measured with 10ms half sine wave pulse and a repetition frequency of 50Hz.

$I_{DRM}$: The maximum repetitive off state forward leakage current given at specified conditions

$I_{RRM}$: The maximum repetitive reverse leakage current given at specified conditions

$V_{RSM}$: The maximum non-repetitive peak value of the voltage in reverse direction e.g. occurring due to switching operations, which must not be exceeded even for shortest pulse duration.

### 2.2 Conducting

| | | | | | |
|---|---|---|---|---|---|
| $I_{T(AV)}$ | Mean on state current | 180° sin,50 Hz,$T_C$= 74°C,Double side cooled | | 2620 | A |
| I | RMS on-state current | | | 4113 | A |
| $I_{TSM}$ | Surge on-state current | Sine wave,10 ms Without reverse voltage | 25 | 38.0 | kA |
| | | | 125 | 37.2 | kA |
| $I^2t$ | $I^2t$ | Sine wave,10 ms Without reverse voltage | 25 | 7220 X $10^3$ | $A^2S$ |
| | | | 125 | 6919 X $10^3$ | $A^2S$ |
| $V_T$ | On-state voltage | On-state current = 4000A | 125 | 2.00 | V |
| $V_{T(TO)}$ | Threshold voltage | | 125 | 1.308 | V |
| $r_T$ | On-state slope resistance | | 125 | 0.170 | mΩ |

$I_{T(AV)}$: The maximum allowable on state current
$I_{RMS}$: The maximum allowable root mean square (RMS) on state current

$I_{T(AV)}$ and $I_{RMS}$ are defined for 180° sine wave pulses of the 50% duty cycle at the case temperature $T_C$

$I_{TSM}$ : The maximum allowable non-repetitive peak on state current

$I^2t$ : The integral of the square of the current over a defined period

$I_{TSM}$ and $I^2t$ are determined for a half sine wave current pulse without a reverse voltage. Above the specified values, the device will fail short-circuit. Both parameters are required for protection coordination.

$V_T$ : The maximum on state voltage drop of the thyristor at given conditions

The threshold voltage, $V_{T(TO)}$, and the slope resistance, $r_T$, allow a linear representation of the thyristor on state voltage drop, and are used to calculate conduction losses of the device, PT. For a given current, the conduction losses can be calculated using equation 1:

$$P_T = I_{TAV} * V_{T(TO)} + I^2_{TRMS} * r_T \qquad \text{Eq.1}$$

To minimise the losses, $V_{T(TO)}$ and $r_T$ should be as low as possible.

## 2.3 Switching characteristics

| | | | | | |
|---|---|---|---|---|---|
| di/dt | Critical rate of on-state current | Repetitive | 125 | 1000 | A/us |
| dv/dt | Critical rate of on-state voltage | $V_{DR}$=67%$V_{DRM}$ | 125 | 500 | V/us |
| Qrr | Recovered Charge | $I_{TM}$=10000A,-$di_r/dt$=60A/us,$V_R$=50V,$T_p$=1000us | 125 | 1800 | uC |
| Tq | Circuit commutated turn off time | $I_{TM}$=10000A,-$di_r/dt$=20A/us,$V_R$=50V,$T_p$=1000us Reapplied dv/dt=200V/us,$V_{DR}$=33%$V_{DRM}$ | 125 | 50 - 70 | us |

di/dt : Critical rate of rise of on state current at specified conditions

dv/dt : Critical rate of rise of off state voltage at specified conditions

$Q_{rr}$ : Recovered charge at specified conditions

$T_q$ : Circuit commutated turn off time is the minimum waiting time between the instant when the main current passes through zero from forward direction to the reverse direction and the earliest begin of a fast rising forward off state volt

To meet the application demand, MS power offered fast switching thyristors with $Q_{rr}/Q_{ra}$ in the band of ± 10% at specified reverse voltage $v_{rm}$ which greatly improve the balancing of voltage among thyristors connected in series at turn off.

## 2.4 Thermal characteristics

| | | | | |
|---|---|---|---|---|
| $R_{th(j-c)}$ | Thermal impedance,sin180° | Junction to case,Double side cooled | 0.008 | °C/W |
| $R_{th(j-c)}$ | Thermal impedance,rec120° | Junction to case,Double side cooled | 0.0092 | °C/W |
| $R_{th(j-c)}$ | Thermal impedance | Junction to case,Double side cooled | 0.003 | °C/W |
| $T_j$ | Max.junction temperature | | 125 | °C |
| $T_{stg}$ | Storage temperature | | -40....125 | °C |

$R_{th(j-c)}$ : The thermal resistance as measured from the thyristors junction to the base plate of thyristor's case

$R_{th(c-h)}$ : The thermal resistance as measured from the thyristor's case to heat sink

The thermal resistances $R_{th(j-c)}$ and $R_{th(c-h)}$ are measures of how well power can be transferred to the cooling system. The values are given for the double side cooling, where the device is clamped between two heat sinks. The temperature rise of the " virtual junction" of the silicon wafer inside the thyristor in relation to the heat sink is given by equation 2.

$$\Delta T_{jh} = P_T * ( R_{th(j-c)} + R_{th(c-h)} ) \qquad \text{Eq. 2}$$

It is preferable that $R_{th(j-c)}$ and $R_{th(c-h)}$ should be as low as possible since the silicon temperature determines the current capability of the thyristor. Furthermore, the temperature excursion of the silicon wafer determines the load-cycling capability and life expectancy of the thyristor.

$T_j$ : The operating junction temperature

$T_{stg}$ : The maximum allowable temperature interval for short term storage of the thyristor without transport box

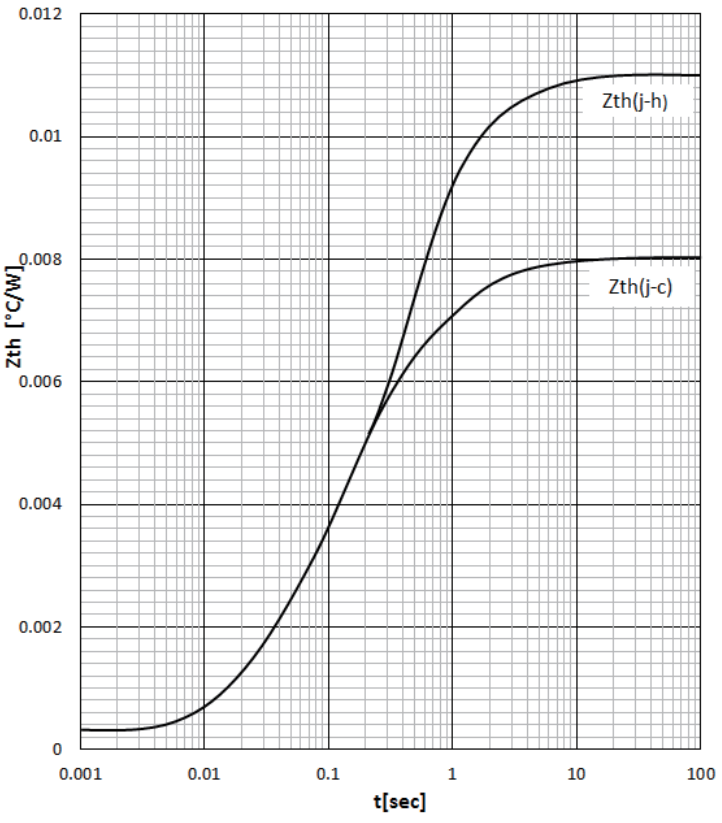



Figure 1: Transient thermal impedance

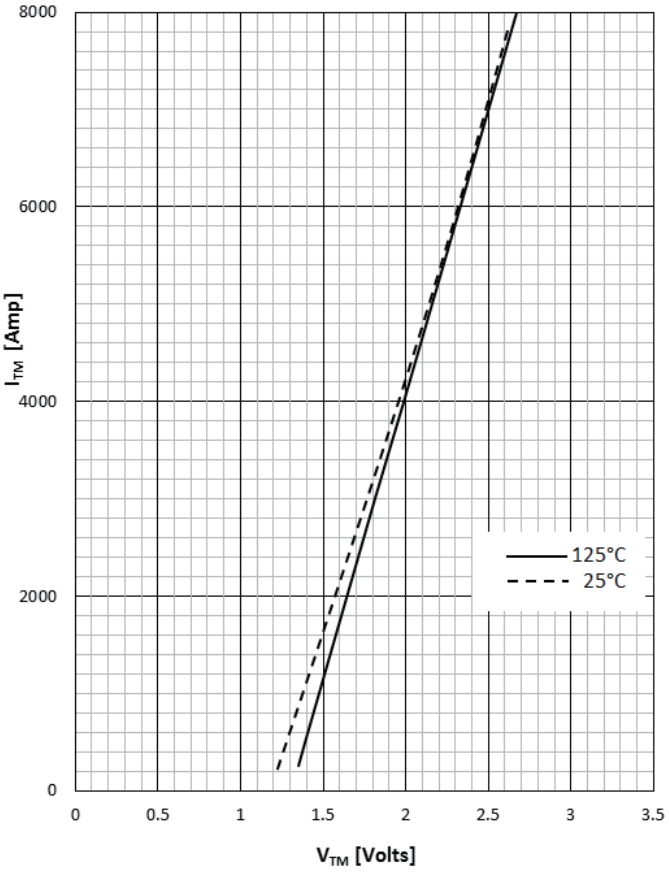



Figure 2: On-state characteristics

## 2.5 Gate trigger characteristics

| | | | | | |
|---|---|---|---|---|---|
| $I_{gt}$ | Gate trigger current | VD=6V | 25 | 300 | mA |
| $V_{gt}$ | Gate trigger voltage | VD=6V | 25 | 3.0 | V |
| $I_H$ | Holding current | VD=6V,gate open circuit | 25 | 1000 | mA |
| $I_L$ | Latching current | VD=6V | 25 | 1200 | mA |

$I_{gt}$ : The value of gate current which causes the thyristor to switch from the off-state to on-state in forward direction. The gate trigger current is dependent on the magnitude of the voltage across the main terminals and the junction temperature.

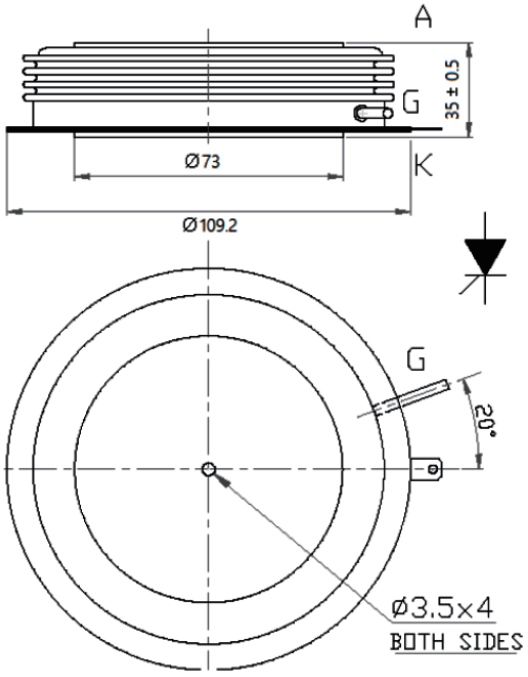
$V_{gt}$ : The voltage which occurs across gate terminal and cathode terminal when the gate current flows

$I_H$ : The minimum Anode to Cathode current required for thyristor to remain in on-state

IL : The minimum Anode to Cathode current required for thyristor to switch from off-state to on-state after application of gate current.

## 2.6 Mechanical

| | | | |
|---|---|---|---|
| M | Clamping Force | 30 - 47 | kN |
| W | Weight (Approx.) | 1750 | gm |




The mechanical part of the data sheet includes the outline drawing of the thyristor housing where all dimensions are in millimetres.

M : The recommended clamping force applied to the device in order to establish the contact pressure for its optimal performance

W : The device weight in grams

## 2.7 Power loss and maximum case temperature characteristics

Figure 3 and 4 show forward power losses, $P_T$, as a function of the average forward current, $I_{T(AV)}$, for typical sine and square current waveform. The curves are calculated based on Eq.1 without considering and turn on, turn off losses.

Figure 5 and 6 describe the maximum permissible case temperature, Tc, against the on state current for typical sine and square current waveforms. The curves are calculated based on the thermal resistance for the double side cooling, for the specified current waveform and at the maximum junction temperature.

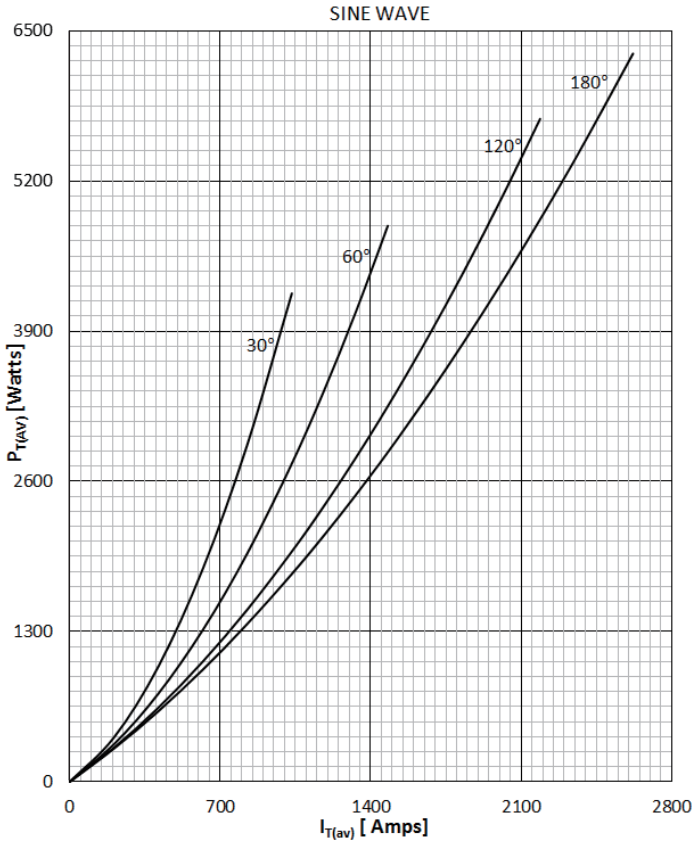



Figure 3 : Dissipation characteristics , sine wave

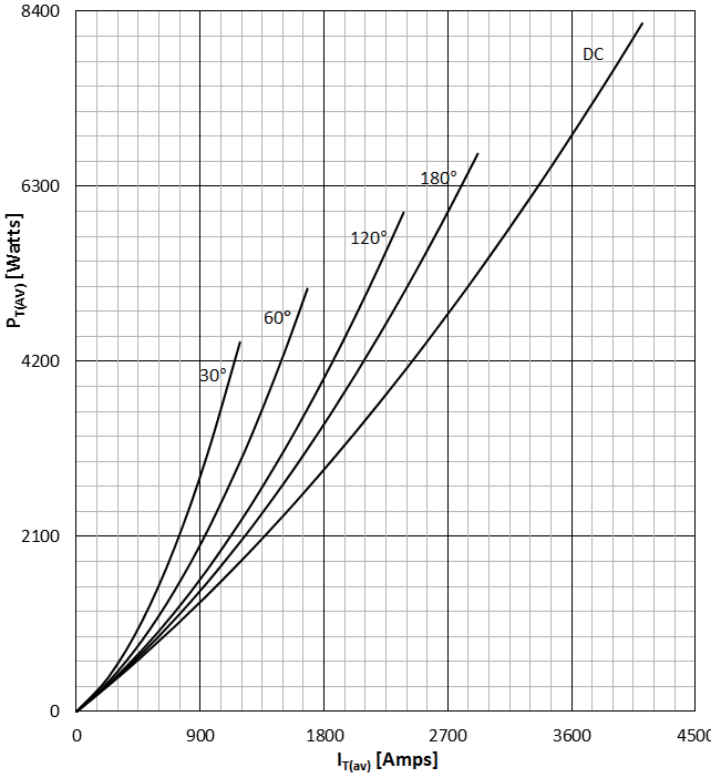



Figure 4 : Dissipation characteristics , square wave

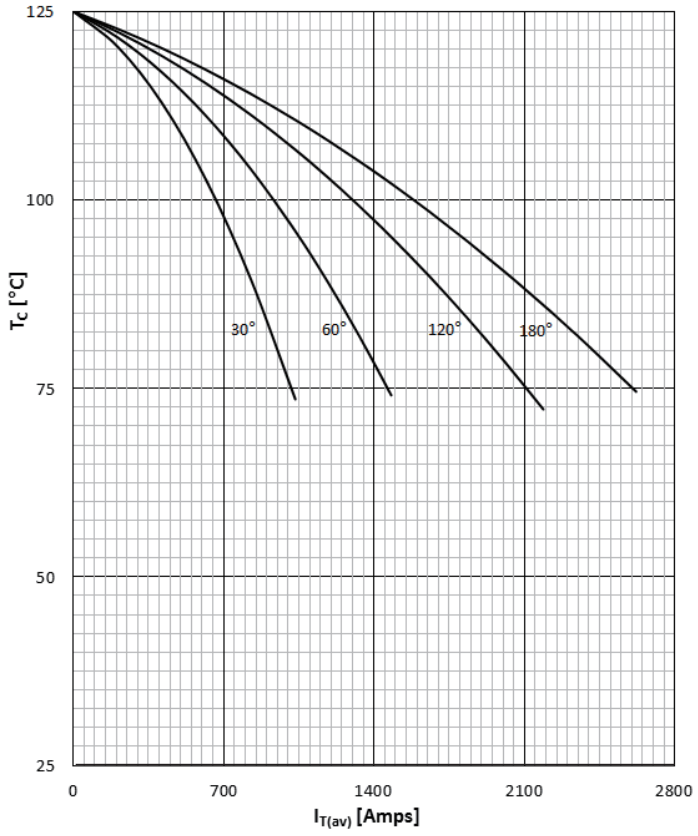



Figure 5 : On-state current derating curve, sine wave

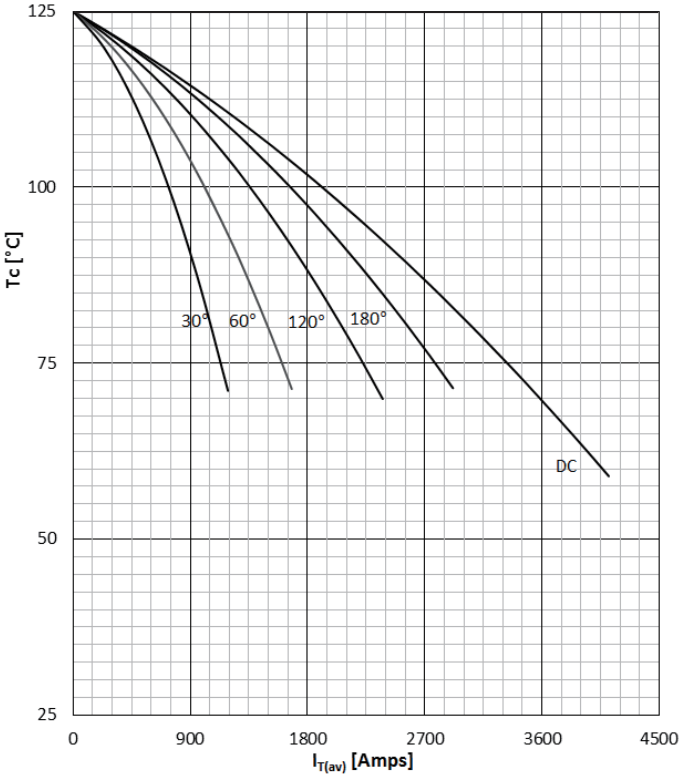



Figure 6 : On-state current derating curve , square wave

## 3. Mounting recommendations

The proper and careful mounting of thyristors is mandatory for reliable and undisturbed operation because both electrical and thermal contacts are produced by fixing the devices in place, e.g. on heat sinks. For this reason, the procedures listed in the following must be closely adhered to.
In the range of the contact areas of thyristor and heat sink, the deviation of flatness and roughness of surfaces must not exceed 10µm. Before mounting, apply a thin layer of suitable thermal joint compound to the contact surface.

### 3.1 Mounting by means of flat spring or clamping plate

Clamping systems for double sided cooling of thyristors between two heatsink halves shall be designed so that they apply the force of spring through the centre line of the thyristor whereas the heat sink halves are brought into contact with the thyristor contact surfaces by alternately tightening the clamp bolts until the full force is reached. The clamping system must be chosen to withstand the required mounting pressure. Mounting instructions given by the manufacturer of the clamping system must be adhered to.

## 3.2 Arrangement of heat sink

Thyristors with heat sinks for force air cooling or water cooling can be mounted in any position as long as the flow rates of the cooling medium will be maintained. In the case of natural convection cooling, the heat sink have to arranged so that their ribs are in vertical position to allow the cooling air to pass unhindered.
Heat sinks are live and, for this reason, have to be mounted electrically insulated.
Heat sinks have to be mounted in a sufficient distance from the bottom or from other equipment. If the number of heat sinks are arranged on top of each other, a sufficiently great spacing has be ensured, in particular at natural convection cooling, to prevent mutual heating up.

# 4 Application aspects - Series connection

When connecting thyristors in series, equal distribution of the off state voltage in steady state condition and dynamic should be aims for. Reasons for deviations from the ideal voltage sharing are:

**• Variance of the gate controlled delay time**
During turn-on the thyristors triggered last are exposed by higher off-state voltage.

**• Different leakage currents**
Without additional external components, an unfavourable voltage sharing may occur during the steady off-state condition in both directions as the voltage across the individual thyristors results out of the uniform reverse current in the series circuit.

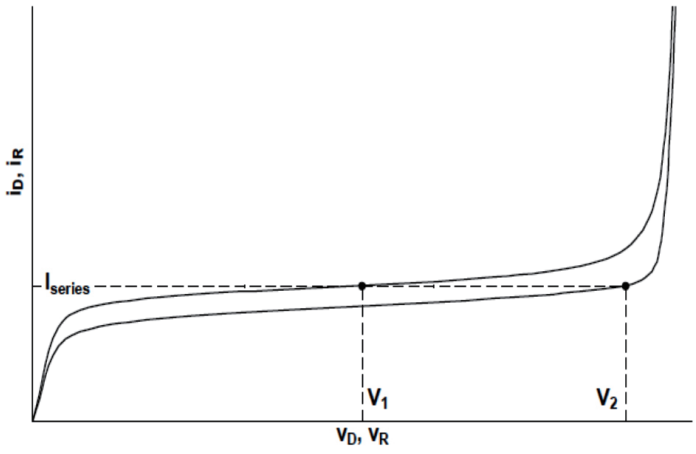



Fig.7: Voltage sharing imbalance due to different leakage current

**• Variance of the reverse recovery charge**
Differences of the reverse recovery charge Qr cause different reverse recovery times trr and peak reverse recovery currents $I_{RM}$ which means that the thyristors take up off-state voltage at different times. The variance of the reverse recovery charge Δ Qr of two thyristors connected in series effects a voltage deviation ΔV ≈ ΔQr/C where C is the capacitor of the parallel snubber circuit.

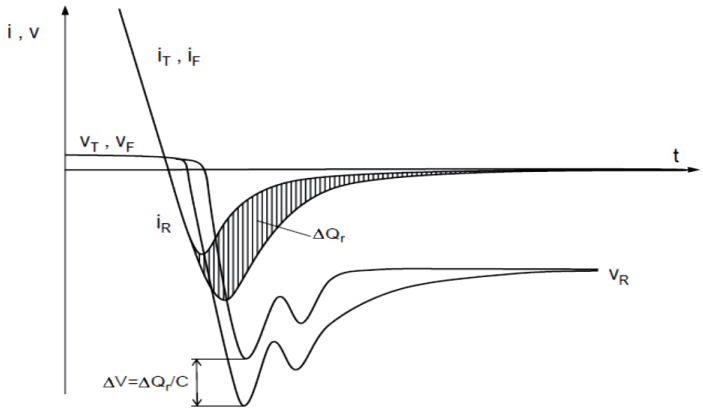



Fig.8 : Voltage sharing imbalance due to different Turn off characteristics

Equal off-state voltage for thyristors connected in series may be achieved by the following measures :

**• Steady state voltage sharing during the off-state phase**
For this the RC-snubber is often sufficient. In case the DC off-state voltage is applied for longer periods, an additional voltage sharing resistor paralleled to each thyristor is necessary. It should carry about two to five times the leakage current of the applied power semiconductor at operating temperature in order to externally force a steady state voltage symmetry. If the operating temperature is less then the maximum allowable junction temperature for continuous operation, the leakage current drops per 10°C to approx. 60% of the initial value.

**• Dynamic voltage sharing at turn-on**
To reduce the variance of the gate controlled delay times, triggering of electrically triggered thyristors is necessary with synchronous, steep and high trigger pulses. $i_{GM} \geq 5...10\ I_{GT}$ $d_{iG}/dt \geq i_{GM}/(0.8\text{-}1\mu s)$. Such strong trigger pulses reduces the spread of the gate controlled delay time to values $\Delta t_{gd} < 1\mu s$. It has to be ensured that the reverse blocking voltage of the thyristor which is last to turn on (in a series connection) increases only slowly. Often the RC-snubber is sufficient for this. In case the inductance of this circuit working jointly with the RC networks are not sufficient to reduce the reverse voltage increase additional saturable inductances are to be implemented.

**• Dynamic voltage sharing at turn-off**
During turn-off it is possible to improve the imbalance of off-state voltage sharing both by sufficient dimensioning of the paralleled snubbers as well as by a small variance of the recovery charge ΔQr of the thyristors in series.

The reverse recovery charge ( $Q_{RR}$ and $Q_{RA}$ ) is a function of both the device design characteristics and the circuit commutation conditions. The Reverse voltage $V_{RM}$, during commutation greatly influence the $Q_{RR}$ and $Q_{RA}$ values.
MS Power Semiconductor has a highly equipped test lab that can test Fast switching thyristors for $Q_{RR}/Q_{RA}$ .
To meet the application demand, MS Power offered Fast switching thyristors with $Q_{RR}/Q_{RA}$ in the band of ± 10% which greatly improve the balancing of voltage among thyristors connected in series at turn off.

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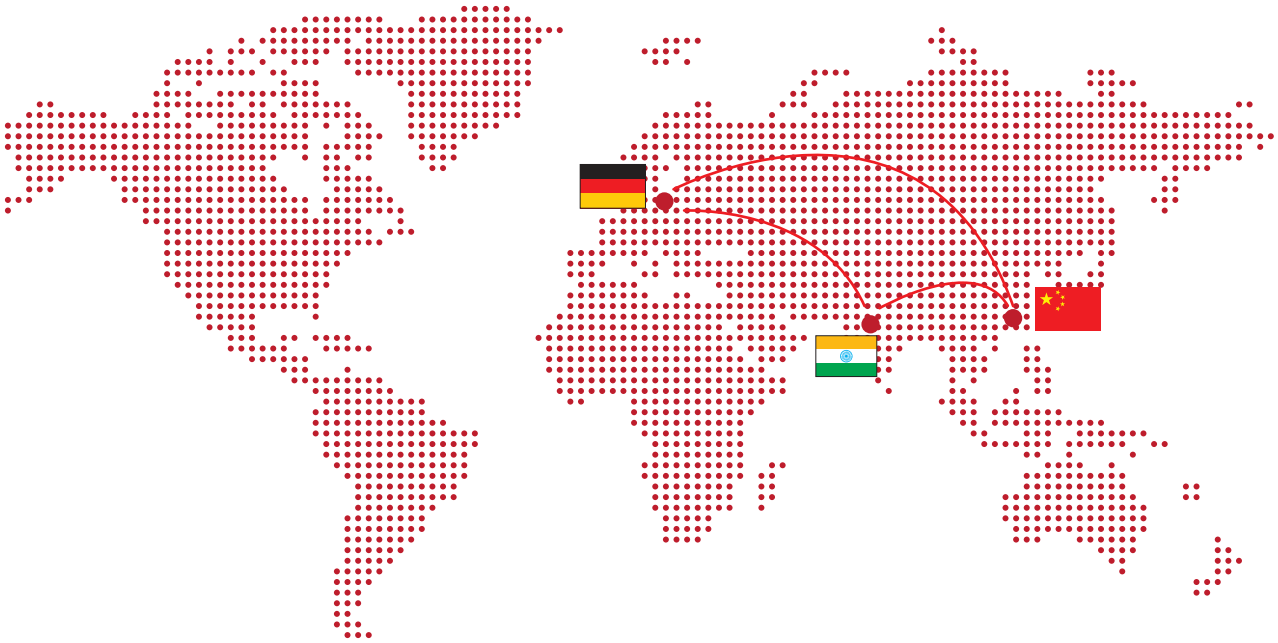
## we provide:

- Discrete Thyristors
- Discrete Diodes
- Power Modules
- Power Bridges
- Power Stack

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